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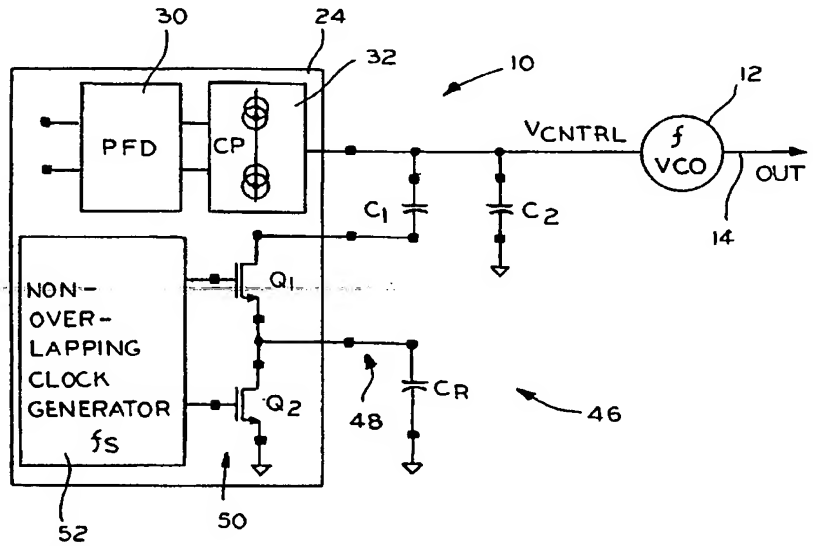
(54) Title: PLL LOOP FILTER WITH SWITCHED-CAPACITOR RESISTOR



(57) Abstract: A phase-locked loop circuit having improved phase noise characteristics includes a voltage-controlled oscillator (12) developing an oscillating output signal responsive to a voltage control input. A reference source provides a reference frequency signal. A phase detector (30) is operatively connected to the voltage-controlled oscillator and the reference source developing an output proportional to a phase difference between the oscillating output signal and the reference frequency signal. A loop filter (46) connects the phase detector output to the voltage control input. The loop filter includes a switched-capacitor equivalent resistor (Q1, Q2, CR).

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PLL Loop Filter With Switched-Capacitor Resistor

FIELD OF THE INVENTION

This invention relates to phase-locked loop filter circuits and, more particularly, to a loop filter with a switched-capacitor resistor.

BACKGROUND OF THE INVENTION

Phase-locked loop circuits are commonly used in circuits that require generation of a high-frequency periodic signal with the frequency of the signal being an accurate multiple of the frequency of a very stable and low-noise reference frequency signal. Phase-locked loop circuits also find applications where the phase of the output signal has to track the phase of the reference signal, thus the name phase-locked loop.

Phase-locked loop circuits are used for generating local oscillator signals in radio receivers and transmitters. The local oscillator signal is used for channel selection and thus is a multiple of a stable, low-noise and often temperature-compensated reference signal generator. Phase-locked loop circuits are also used for clock recovery applications in digital communication systems, disk-drive read-channels and the like. Phase-locked loop circuits are also used in frequency modulators and in the de-modulation of frequency-modulated signals. An overview of typical applications is discussed in "Monolithic Phase-Locked Loops and Clock Recovery Circuits, Theory and Design", Behzad Razavi, IEEE Press, 1996.

A typical phase-locked loop circuit includes a loop filter connecting a phase detector to a voltage-controlled oscillator. The loop filter defines the dynamics of the phase-locking feedback loop such that certain stability criteria are fulfilled and the loop doesn't enter an oscillatory condition. In second and higher order phase-locked loop circuits, this stabilization is commonly achieved by inserting a resistor into the loop filter. The resistor generates thermal noise that amounts to a contribution to the phase noise spectrum of the phase-locked

loop output signal. The loop filter resistor noise can dominate the overall phase noise in the neighborhood of the loop band width.

The present invention is directed to overcoming one or more of the problems discussed above in a novel and simple manner.

SUMMARY OF THE INVENTION

In accordance with the invention there is provided a phase-locked loop circuit including a loop filter with a switch-capacitor resistor.

Broadly, there is disclosed herein a phase-locked loop circuit having improved phase noise characteristics including a voltage-controlled oscillator developing an oscillating output signal responsive to a voltage control input. A reference source provides a reference frequency signal. A phase detector is operatively connected to the voltage-controlled oscillator and the reference source developing an output proportional to a phase difference between the oscillating output signal and the reference frequency signal. A loop filter connects the phase detector output to the voltage control input. The loop filter includes a capacitor and a switching circuit. The switching circuit alternately connects the capacitor to the phase detector output and to ground.

It is a feature of the invention that the loop filter further comprises a second capacitor connected between the switching circuit and the phase detector output and an additional capacitor connected between the phase detector output and ground.

It is another feature of the invention that the switching circuit comprises a first transistor connecting the capacitor to the phase detector output and a second transistor connecting the capacitor to ground. The switching circuit further comprises a non-overlapping clock generator circuit for controlling the first and second transistors. The clock generator circuit operates at a frequency above a loop bandwidth of the phase-locked loop circuit.

It is an additional feature of the invention that the phase detector comprises a phase frequency detector. The phase detector also includes a

charge pump circuit and the loop filter converts current pulses from the charge pump circuit into a voltage at the voltage control input. The phase detector includes a pair of edge-triggered resettable flip-flops and the oscillating output signal and the reference frequency signal are clock signals for the flip-flops and the flip-flops drive the charge pump circuit.

It is yet another feature of the invention to provide dividers connecting the oscillating output signal and the reference frequency signal to the phase detector.

There is disclosed in accordance with another aspect of the invention a phase-locked loop circuit including a voltage-controlled oscillator developing an oscillating output signal responsive to a voltage control input. A reference source provides a reference frequency signal. A phase frequency detector is operatively connected to the voltage-controlled oscillator and the reference source developing an output having positive or negative current pulses having widths proportional to a phase difference between the oscillating output signal and the reference frequency signal. A loop filter connects the phase detector output to the voltage control input. The loop filter includes an integrator converting current pulses into a voltage at the voltage control input and comprising a capacitor and a switching circuit. The switching circuit alternately connects the capacitor to the phase detector output and to ground.

Further features and advantages of the invention will be readily apparent from the specification and from the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a phase-locked loop circuit;

Fig. 2 is a block diagram of a phase frequency detector and charge pump circuit of the circuit of Fig. 1;

Fig. 3 is a block diagram illustrating a portion of the phase-locked loop circuit of Fig.1 including a schematic with a prior art loop filter circuit;

Fig. 4 is a block diagram illustrating a portion of the phase-locked loop circuit of Fig. 1 including a schematic with a loop filter circuit in accordance with the invention; and

Fig. 5 is a curve illustrating spectral noise voltage density for a switched-capacitor resistor.

DETAILED DESCRIPTION OF THE INVENTION

Referring initially to Fig. 1, a typical implementation of a phase-locked loop circuit 10 may be used for generating local oscillator signals in a radio receiver or a transmitter, such as in cellular telephones. The circuit 10 includes a voltage-controlled oscillator (VCO) 12 developing an oscillating output signal on a line 14 responsive to a voltage control input on a line 16. A reference source 18 provides a reference frequency signal on a line 20. The reference frequency signal on the line 20 is coupled via a first divider 22 to one input of a phase detector 24. The oscillating output signal on the line 14 is connected through a second divider 26 to a second input of the phase detector 24. Particularly, the reference frequency signal is divided by a reference division ratio R. Similarly, the oscillating output signal is divided by a main division ratio N.

The phase detector 24 provides an output signal that is proportional to a phase difference of its two input signals. A loop filter 28 filters the phase detector output signal to develop the voltage control signal on the line 16.

Depending on the circuit implementation, the phase detector 24 may comprise a phase-frequency detector. In the illustrated embodiment of the invention, the phase detector 24 comprises a combination of a phase frequency detector 30 and charge pump circuit 32, as illustrated in Fig. 2.

The phase frequency detector 32 is implemented as a digital circuit consisting of two edged-triggered resettable D-type flip-flops 34 and 36 with

their D inputs connected to logical 1. The reference signal, labeled REF, from the divider 22 acts as the clock signal to the first flip-flop 34. The oscillating signal, labeled VCO, from the divider 26 acts as a clock signal to the second flip-flop 36. The output of the first flip-flop 34 comprises an "UP" output. The output of the second flip-flop 36 comprises a down or "DN" output. The outputs of the flip-flops 34 and 36 are also connected to the inputs of an AND gate 38. The output of the AND gate 38 is connected to the reset inputs of the flip-flops 34 and 36.

The operation of the pulse-frequency detector 30 is such that the up output is set to logical 1 by the REF edge if it arrives prior to the VCO edge. The later VCO edge will reset the UP output back to logical 0. The DN output is set to logical 1 if the VCO edge arrives prior to the REF edge and is then reset to 0 by the later REF edge. Logical 1s on the UP and DN outputs enable the charge pump circuit 32, as described below so that either positive or negative current pulses arrive at the charge pump output, labeled CPOUT. The width of these pulses is proportional to the phase difference of the REF and VCO signals.

The charge pump circuit 32 comprises first and second current reference sources 40 and 42 series connected between supply and ground. The first current source 40 is operated by the UP output. The second current source is operated by the DN output. The junction between the current sources 40 and 42 carries the charge pump output current, CPOUT.

The purpose of the phase-locked loop circuit 10 of Fig. 1 is to set the output frequency of the voltage-controlled oscillator 12 and achieve phase-lock with the reference signal from the source 18. In the implementation of the phase detector 24 of Fig. 1, the current pulses at the charge pump output need to be integrated and converted into a voltage that can be applied to the voltage control input of the oscillator 12. This conversion is implemented by the loop filter 28. In addition to functioning as an integrator, the loop filter 28 also determines the stability of the feedback loop.

Referring to Fig. 3, a portion of the phase-locked loop circuit 10 of Fig. 1 is illustrated utilizing a prior art loop filter circuit 44. The loop filter circuit 44 is a network consisting of a series-connected capacitor C_1 and resistor R_1 connected between the charge pump output and ground, and in parallel with a second capacitor C_2. As is known, if the value of the second capacitor C_2 is 0, then the loop filter 44 is second order. Otherwise, the loop filter is a third-order filter.

The value of the resistor R_1 has to be set such that a desired value for a damping factor is achieved. Typically, the damping factor is close to $1/\sqrt{2}$ of the critically damped case. If R_1 were chosen to be 0, then the loop would enter an undamped oscillation with the frequency of oscillation being the natural frequency of the loop, as is known.

While the resistor R_1 and the loop filter 44 is essential for stable loop dynamics, it gives rise to various disadvantages. The loop filter resistor R_1 creates a thermal noise voltage at the oscillator's voltage control input and thus modulates the phase of the VCO 12 in a random fashion. For small frequencies the loop filter's resistor noise is greatly attenuated. As frequency increases, the resistor's phase noise contribution increases. For large tuning sensitivities in small loop bandwidths, the contribution of the loop filter resistor R_1 for the overall output phase noise is significant. Particularly, the loop filter resistor R_1 dominates the overall phase noise in the neighborhood of the loop bandwidth.

A further disadvantage of the prior art loop filter 44 is that over time the supply voltage that supplies the phase-locked loop circuit 10 and the voltage-controlled oscillator 12 decreases. To keep the same frequency tuning range for the output signal with a lower available swing for the VCO control voltage requires that the tuning sensitivity of the VCO 12 be increased. This degrades the achievable phase noise. Thus it is harder to meet phase noise requirements for lower supply voltage implementations of the frequency synthesis blocks.

In accordance with the invention, the functionality of the resistor in a loop filter is implemented without adding the amount of noise that a resistor adds. This allows the same dynamics of a phase-locked loop circuit to be achieved while lowering phase noise. Particularly, it is desirable to lower the contribution of noise to the point where other noise sources in a loop dominate and ultimately limit the performance.

Referring to Fig. 4, a portion of the phase-locked loop circuit 10 of Fig. 1 is illustrated utilizing a loop filter 46 in accordance with the invention. The loop filter circuit 46 uses the capacitors C_1 and C_2 as in Fig. 3. However, the resistor R_1 is replaced with a switched-capacitor equivalent resistor circuit 48. The circuit 48 includes a capacitor C_R and a switching circuit 50.

The preferred application of the phase-locked loop circuit 10 is in conjunction with an application specific integrated circuit (ASIC). Nevertheless, the phase-locked loop circuit 10 could be used with other applications.

For a switched-capacitor equivalent generally, a capacitor C can be assumed to be connected to a source for the time $m*T$. The charge flowing to the capacitor will build up voltage V across it according to $Q = C*V$. Then, the capacitor is disconnected from the source and for the time $(1-m)*T$ the capacitor is discharged. Therefore, during the time T, the charge $Q = C*V$ was transferred out of the source. Hence, the average current is: $I = Q/T = V/(T/C)$ and the arrangement implements an equivalent resistor value of

$$R = \frac{T}{C}$$

In order for the averaging to be accurate, it is necessary that the sampling frequency, namely $f_s = 1/T$, is well above the frequency of the signal delivered by the source. Also, it is necessary that the capacitor can be fully discharged during the time $(1-m)*T$, otherwise the equivalent resistance differs from $R = T/C$. The equivalent resistor value does not depend on the switching duty cycle m.

The resistor implementation described above is only useful if the amount of noise generated by the circuit is below the noise level of the conventional resistor as shown in Fig. 3. For the time interval $(1-m)*T$, the capacitor is shorted and the rms-noise voltage across its terminals can be shown to be $v^2_{RMS}=kT/C$. At the time the switch is flipped to connect the capacitor to the source, the momentary noise voltage across the capacitor's terminals is sampled and will not change until the cycle starts again. Since it is necessary that the capacitor fully discharges during the time $(1-m)*T$, the sampling frequency f_s does not fulfill the Nyquist criterion with respect to the bandwidth of the noise spectrum across the capacitor's terminals and strong aliasing will occur. Therefore, the entire noise power is being folded into the frequency range $-f_s/2 \le f \le f_s/2$ with the spectral density $kT/(f_sC)$. The spectrum of the sampled and held (for the time $m*T$) noise voltage is then (using $R=1/(f_sC)$):

$$\overline{v_{SH}^2(f)} = 4kTR \cdot \frac{m^2}{2} \cdot \sin c^2\left(\pi m \frac{f}{f_s}\right).$$

Fig. 5 shows the spectral noise voltage density for an equivalent 10kΩ resistor, $f_s=1$MHz and $m=0.5$.

The switching circuit 50 that connects the capacitor C_R to the rest of the loop filter 46 or to ground is implemented via switches in the form of MOS transistors Q_1 and Q_2. The switches Q_1 and Q_2 are controlled by a non-overlapping clock generator 52 that is being driven by a signal source with frequency f_s and a duty cycle m. The switching control is such that the first transistor Q_1 is on for the time m/f_s and the second transistor Q_2 is on for the time $(1-m)/f_s$. If the switching frequency f_s is chosen well above the loop bandwidth of the phase-locked loop circuit 10 and $C_R=1/(R_1f_s)$, then the loop filter 46 is equivalent to the loop filter 44 shown in Fig. 3

The capacitor C_1 is connected between the phase detector output and a collector of the transistor Q_1. The emitter of the first transistor Q_1 is

connected to the collector of the second transistor Q_2. The emitter of the second transistor Q_2 is connected to ground. The capacitor C_R is connected to the junction of the transistors Q_1 and Q_2 and to ground. The bases of the transistors Q_1 and Q_2 are connected to the non-overlapping clock generator 52.

The disclosed loop filter circuit 46 produces an equivalent resistor's phase noise contribution well below the total phase noise level as compared to the loop filter 44 of Fig. 3. As a result, other noise sources dominate the noise behavior of the loop.

While the loop filter 46 is disclosed in connection with a digital phase-lock loop circuit using a phase-frequency detector 30 and charge pump 32, the loop filter 46 could be used in connection with other types of phase detector implementations and phase-lock loop circuits, as is apparent.

Thus, in accordance with the invention, there is provided a phase-locked loop filter with a switch-capacitor resistor to improve phase noise characteristics of the output signal generated by the phase-locked loop circuit.

I claim:

CLAIMS

1. A phase-locked loop circuit having improved phase noise characteristics comprising:

a voltage-controlled oscillator developing an oscillating output signal responsive to a voltage control input;

a reference source providing a reference frequency signal;

a phase detector operatively connected to the voltage-controlled oscillator and the reference source developing an output proportional to a phase difference between the oscillating output signal and the reference frequency signal; and

a loop filter connecting the phase detector output to the voltage control input, the loop filter including a capacitor and a switching circuit, the switching circuit alternately connecting the capacitor to the phase detector output and to ground.

2. The phase-locked loop circuit of claim 1 wherein the loop filter further comprises a second capacitor connected between the switching circuit and the phase detector output.

3. The phase-locked loop circuit of claim 1 wherein the loop filter further comprises an additional capacitor connected between the phase detector output and ground.

4. The phase-locked loop circuit of claim 1 wherein the switching circuit comprises a first transistor connecting the capacitor to the phase detector output and a second transistor connecting the capacitor to ground.

5. The phase-locked loop circuit of claim 4 wherein the switching circuit further comprises a non-overlapping clock generator circuit for controlling the first and second transistors.

6. The phase-locked loop circuit of claim 5 wherein the clock generator circuit operates at a frequency above a loop bandwidth of the phase-locked loop circuit.

7. The phase-locked loop circuit of claim 1 wherein the phase detector comprises a phase frequency detector.

8. The phase-locked loop circuit of claim 1 wherein the phase detector includes a charge pump circuit and the loop filter converts current pulses from the charge pump circuit into a voltage at the voltage control input.

9. The phase-locked loop circuit of claim 8 wherein the phase detector includes a pair of edge-triggered resettable flip-flops and the oscillating output signal and the reference frequency signal are clock signals for the flip-flops and the flip-flops drive the charge pump circuit.

10. The phase-locked loop circuit of claim 1 further comprising dividers connecting the oscillating output signal and the reference frequency signal to the phase detector.

11. A phase-locked loop circuit having improved phase noise characteristics comprising:

a voltage-controlled oscillator developing an oscillating output signal responsive to a voltage control input;

a reference source providing a reference frequency signal;

a phase frequency detector operatively connected to the voltage-controlled oscillator and the reference source developing an output having positive or negative current pulses having pulse widths proportional to a phase difference between the oscillating output signal and the reference frequency signal; and

a loop filter connecting the phase detector output to the voltage control input, the loop filter including an integrator converting current pulses into a voltage at the voltage control input and comprising a capacitor and a switching circuit, the switching circuit alternately connecting the capacitor to the phase detector output and to ground.

12. The phase-locked loop circuit of claim 11 wherein the integrator further comprises a second capacitor connected between the switching circuit and the phase detector output.

13. The phase-locked loop circuit of claim 11 wherein the integrator further comprises an additional capacitor connected between the phase detector output and ground.

14. The phase-locked loop circuit of claim 11 wherein the switching circuit comprises a first transistor connecting the capacitor to the phase detector output and a second transistor connecting the capacitor to ground.

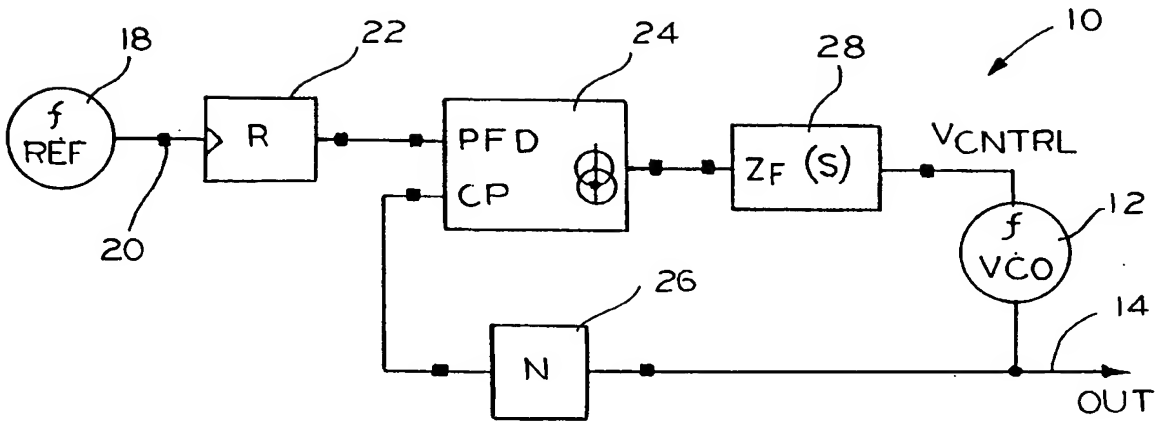
15. The phase-locked loop circuit of claim 14 wherein the switching circuit further comprises a non-overlapping clock generator circuit for controlling the first and second transistors.

16. The phase-locked loop circuit of claim 15 wherein the clock generator circuit operates at a frequency above a loop bandwidth of the phase-locked loop circuit.

17. The phase-locked loop circuit of claim 11 wherein the phase frequency detector includes a charge pump circuit.

18. The phase-locked loop circuit of claim 17 wherein the phase frequency detector includes a pair of edge-triggered resettable flip-flops and the oscillating output signal and the reference frequency signal are clock signals for the flip-flops and the flip-flops drive the charge pump circuit.

19. The phase-locked loop circuit of claim 11 further comprising dividers connecting the oscillating output signal and the reference frequency signal to the phase frequency detector.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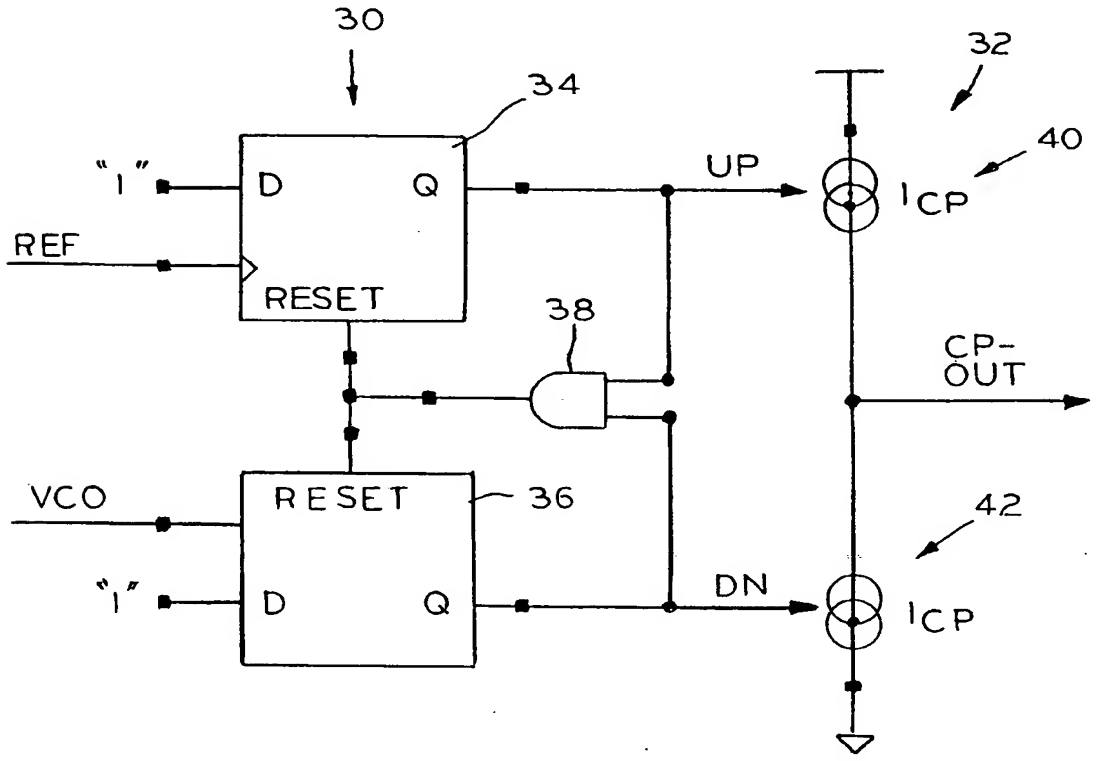
22
24
28
10
f REF
R
PFD
CP
ZF (S)
VCNTRL
20
12
f VCO
26
14
N
OUT

FIG.1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D
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ICP

FIG.2

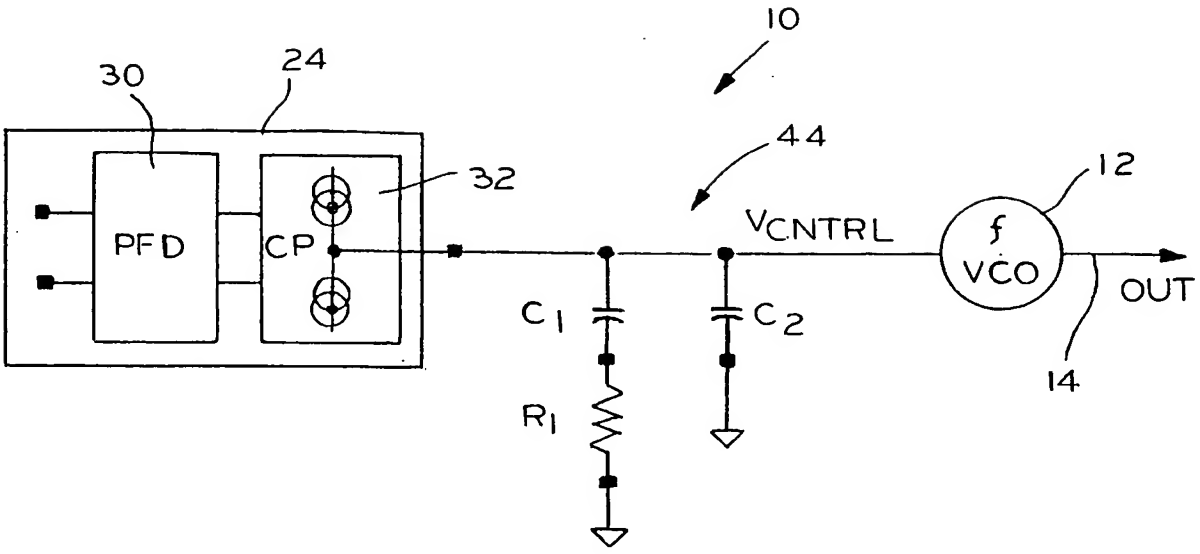

FIG.3
PRIOR ART

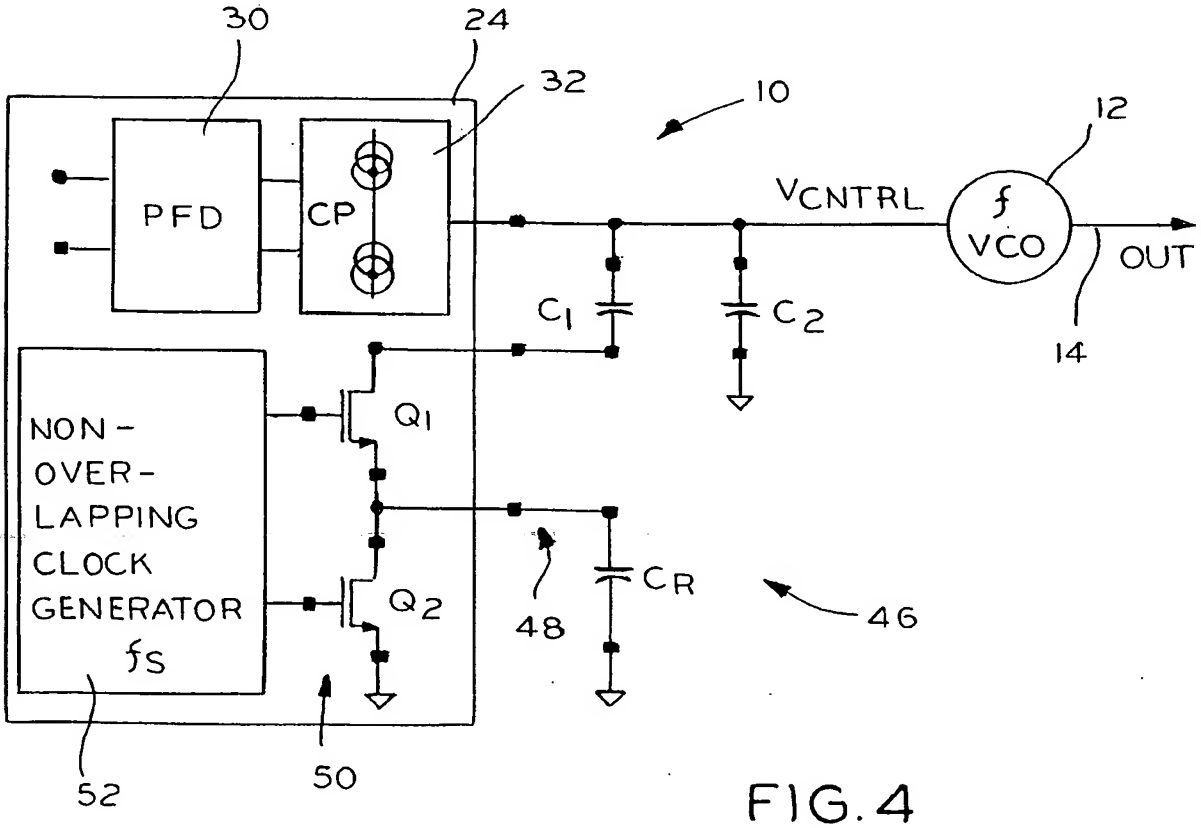

FIG.4

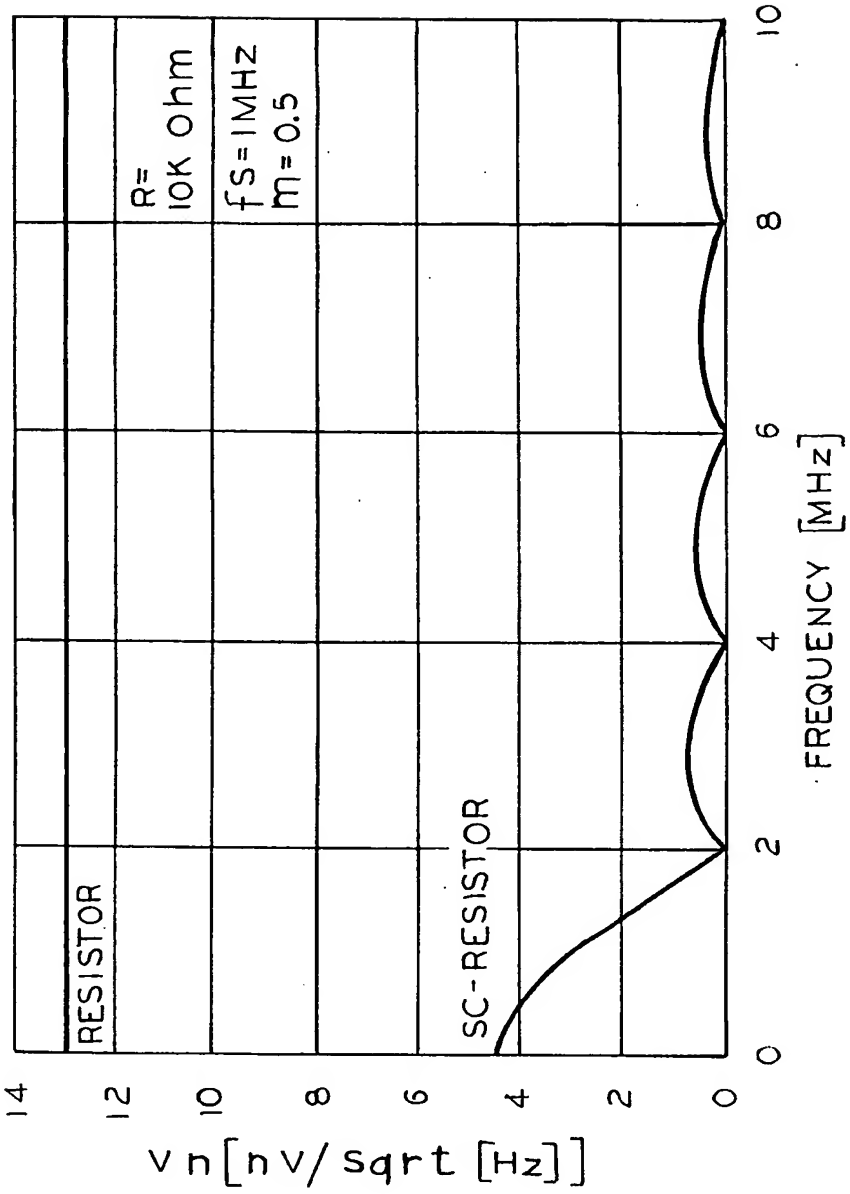
R=
10K Ohm
fS=1MHz
m=0.5
RESISTOR
SC-RESISTOR
14
12
10
8
6
4
2
0
Vn[nV/sqrt[Hz]]
0
2
4
6
8
10
FREQUENCY [MHz]

FIG. 5

INTERNATIONAL SEARCH REPORT

Intern .ial Application No
PCT/US 00/25929

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/093

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, COMPENDEX, EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 023 (E-705), 19 January 1989 (1989-01-19) & JP 63 227120 A (MATSUSHITA ELECTRIC IND CO LTD), 21 September 1988 (1988-09-21) abstract; figures 1,2A,2B	1,4,5,10
Y		7-9,11, 14-19
Y	US 5 055 803 A (HIETALA ALEXANDER W) 8 October 1991 (1991-10-08) column 1, line 6 - line 60; figures 1,6	7-9,11, 14-19

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 December 2000	16/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Balbinot, H

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INTERNATIONAL SEARCH REPORT

Intern .ial Application No
PCT/US 00/25929

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ASTA D ET AL: "ANALYSIS OF A HYBRID ANALOG/SWITCHED-CAPACITOR PHASE-LOCKED LOOP" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS,US,IEEE INC. NEW YORK, vol. 37, no. 2, 1 February 1990 (1990-02-01), pages 183-197, XP000127770 page 183, column 1, line 1 -page 184, column 1, line 7; figures 1-3,7 ---	1,11
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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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